NCP1200

PWM Current-Mode Controller for Low-Power Universal Off-Line Supplies

Housed in SOIC-8 or PDIP-8 package, the NCP1200 represents a major leap toward ultra-compact Switchmode Power Supplies. Due to a novel concept, the circuit allows the implementation of a complete offline battery charger or a standby SMPS with few external components. Furthermore, an integrated output short- circuit protection lets the designer build an extremely low-cost AC-DC wall adapter associated with a simplified feedback scheme.

With an internal structure operating at a fixed 40 kHz, 60 kHz or 100 kHz, the controller drives low gate-charge switching devices like an IGBT or a MOSFET thus requiring a very small operating power. Due to current-mode control, the NCP1200 drastically simplifies the design of reliable and cheap offline converters with extremely low acoustic generation and inherent pulse-by-pulse control.

When the current setpoint falls below a given value, e.g. the output power demand diminishes, the IC automatically enters the skip cycle mode and provides excellent efficiency at light loads. Because this occurs at low peak current, no acoustic noise takes place.

Finally, the IC is self-supplied from the DC rail, eliminating the need of an auxiliary winding. This feature ensures operation in presence of low output voltage or shorts.

Features

- No Auxiliary Winding Operation
- Internal Output Short-Circuit Protection
- Extremely Low No-Load Standby Power
- Current-Mode with Skip-Cycle Capability
- Internal Leading Edge Blanking
- 250 mA Peak Current Source/Sink Capability
- Internally Fixed Frequency at 40 kHz, 60 kHz and 100 kHz
- Direct Optocoupler Connection
- Built-in Frequency Jittering for Lower EMI
- SPICE Models Available for TRANsient and AC Analysis
- Internal Temperature Shutdown
- Pb-Free Packages are Available

Typical Applications

- AC-DC Adapters
- Offline Battery Chargers
- Auxiliary/Ancillary Power Supplies (USB, Appliances, TVs, etc.)

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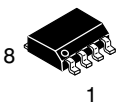
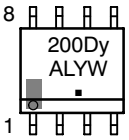
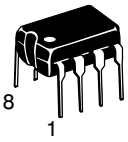
MARKING DIAGRAMS

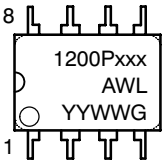


SOIC-8
D SUFFIX
CASE 751



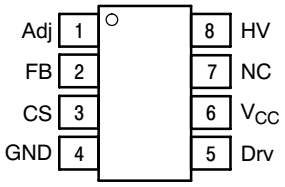


PDIP-8
P SUFFIX
CASE 626



xxx	= Device Code: 40, 60 or 100
y	= Device Code: 4 for 40 6 for 60 1 for 100
A	= Assembly Location
L	= Wafer Lot
Y, YY	= Year
W, WW	= Work Week
G, ▪	= Pb-Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 14 of this data sheet.

Publication Order Number:
NCP1200/D

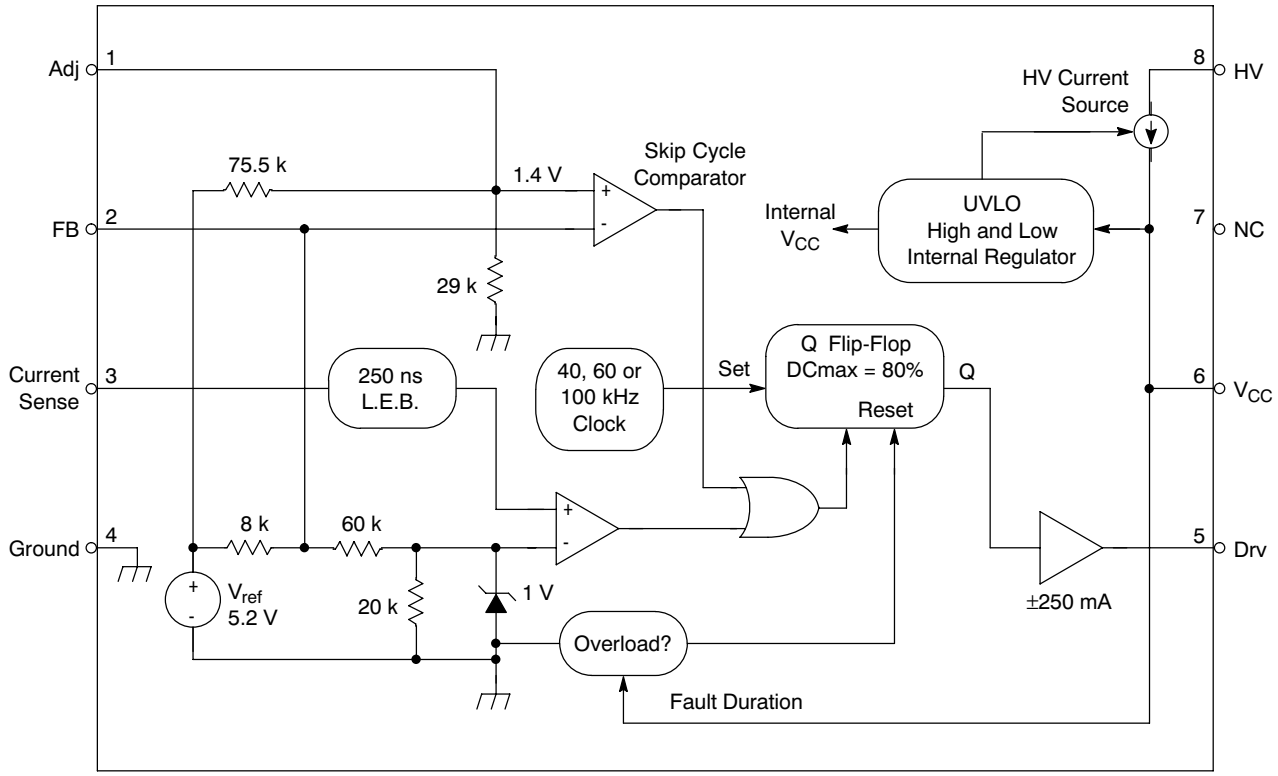


Figure 2. Internal Circuit Architecture

MAXIMUM RATINGS

Rating	Symbol	Value	Units
Power Supply Voltage	V_{CC}	16	V
Thermal Resistance Junction-to-Air, PDIP-8 version Thermal Resistance Junction-to-Air, SOIC version Thermal Resistance Junction-to-Case	$R_{\theta JA}$ $R_{\theta JA}$ $R_{\theta JC}$	100 178 57	°C/W
Maximum Junction Temperature Typical Temperature Shutdown	T_{Jmax} -	150 140	°C
Storage Temperature Range	T_{stg}	-60 to +150	°C
ESD Capability, HBM Model (All Pins except V_{CC} and HV)	-	2.0	kV
ESD Capability, Machine Model	-	200	V
Maximum Voltage on Pin 8 (HV), pin 6 (V_{CC}) Grounded	-	450	V
Maximum Voltage on Pin 8 (HV), Pin 6 (V_{CC}) Decoupled to Ground with 10 μF	-	500	V
Minimum Operating Voltage on Pin 8 (HV)	-	30	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

ELECTRICAL CHARACTERISTICS (For typical values T_J = +25°C, for min/max values T_J = -25°C to +125°C, Max T_J = 150°C, V_{CC}= 11 V unless otherwise noted)

Rating	Pin	Symbol	Min	Typ	Max	Unit
DYNAMIC SELF-SUPPLY (All Frequency Versions, Otherwise Noted)						
V_{CC} Increasing Level at Which the Current Source Turns-of f	6	V_{CCOFF}	10.3	11.4	12.5	V
V_{CC} Decreasing Level at Which the Current Source Turns- on	6	V_{CCON}	8.8	9.8	11	V
V_{CC} Decreasing Level at Which the Latchoff Phase Ends	6	$V_{CClatch}$	-	6.3	-	V
Internal IC Consumption, No Output Load on Pin 5	6	I_{CC1}	-	710	880 Note 1	μA
Internal IC Consumption, 1 nF Output Load on Pin 5, F_{SW} = 40 kHz	6	I_{CC2}	-	1.2	1.4 Note 2	mA
Internal IC Consumption, 1 nF Output Load on Pin 5, F_{SW} = 60 kHz	6	I_{CC2}	-	1.4	1.6 Note 2	mA
Internal IC Consumption, 1 nF Output Load on Pin 5, F_{SW} = 100 kHz	6	I_{CC2}	-	1.9	2.2 Note 2	mA
Internal IC Consumption, Latchoff Phase	6	I_{CC3}	-	350	-	μA
INTERNAL CURRENT SOURCE						
High-voltage Current Source, V_{CC} = 10 V	8	I_{C1}	2.8	4.0	-	mA
High-voltage Current Source, V_{CC} = 0 V	8	I_{C2}	-	4.9	-	mA
DRIVE OUTPUT						
Output Voltage Rise-time @ CL = 1 nF, 10-90% of Output Signal	5	T_r	-	67	-	ns
Output Voltage Fall-time @ CL = 1 nF, 10-90% of Output Signal	5	T_f	-	28	-	ns
Source Resistance (drive = 0, Vgate = V_{CCHMAX} - 1 V)	5	R_{OH}	27	40	61	Ω
Sink Resistance (drive = 11 V, Vgate = 1 V)	5	R_{OL}	5	12	25	Ω
CURRENT COMPARATOR (Pin 5 Un-loaded)						
Input Bias Current @ 1 V Input Level on Pin 3	3	I_{IB}	-	0.02	-	μA
Maximum internal Current Setpoint	3	I_{Limit}	0.8	0.9	1.0	V
Default Internal Current Setpoint for Skip Cycle Operation	3	I_{Lskip}	-	350	-	mV
Propagation Delay from Current Detection to Gate OFF State	3	T_{DEL}	-	100	160	ns
Leading Edge Blanking Duration	3	T_{LEB}	-	230	-	ns
INTERNAL OSCILLATOR (V_{CC} = 11 V, Pin 5 Loaded by 1 kΩ)						
Oscillation Frequency, 40 kHz Version	-	f_{OSC}	36	42	48	kHz
Oscillation Frequency, 60 kHz Version	-	f_{OSC}	52	61	70	kHz
Oscillation Frequency, 100 kHz Version	-	f_{OSC}	86	103	116	kHz
Built-in Frequency Jittering, F_{SW} = 40 kHz	-	f_{jitter}	-	300	-	Hz/V
Built-in Frequency Jittering, F_{SW} = 60 kHz	-	f_{jitter}	-	450	-	Hz/V
Built-in Frequency Jittering, F_{SW} = 100 kHz	-	f_{jitter}	-	620	-	Hz/V
Maximum Duty Cycle	-	Dmax	74	80	87	%
FEEDBACK SECTION (V_{CC} = 11 V, Pin 5 Loaded by 1 kΩ)						
Internal Pullup Resistor	2	Rup	-	8.0	-	kΩ
Pin 3 to Current Setpoint Division Ratio	-	Iratio	-	4.0	-	-
SKIP CYCLE GENERATION						
Default skip mode level	1	Vskip	1.1	1.4	1.6	V
Pin 1 internal output impedance	1	Zout	-	25	-	kΩ

1. Max value @ T_J = -25°C.
2. Max value @ T_J = 25°C, please see characterization curves.

If the leakage inductance is kept low, the MTD1N60E can withstand *accidental* avalanche energy, e.g. during a high-voltage spike superimposed over the mains, without the help of a clamping network. If this leakage path permanently forces a drain-source voltage above the MOSFET BVdss (600 V), a clamping network is mandatory and must be built around Rclamp and Clamp. Dclamp shall react extremely fast and can be a MUR160 type. To calculate the component values, the following formulas will help you:

$$R_{clamp} = \frac{2 \cdot V_{clamp} \cdot (V_{clamp} - (V_{out} + Vf\ sec) \cdot N)}{L_{leak} \cdot Ip^2 \cdot Fsw}$$

$$C_{clamp} = \frac{V_{clamp}}{V_{ripple} \cdot Fsw \cdot R_{clamp}}$$

with:

V_{clamp}: the desired clamping level, must be selected to be between 40 V to 80 V above the reflected output voltage when the supply is heavily loaded.

V_{out} + Vf: the regulated output voltage level + the secondary diode voltage drop

L_{leak}: the primary leakage inductance

N: the Ns:Np conversion ratio

F_{SW}: the switching frequency

V_{ripple}: the clamping ripple, could be around 20 V

Another option lies in implementing a snubber network which will damp the leakage oscillations but also provide more capacitance at the MOSFET's turn-off. The peak voltage at which the leakage forces the drain is calculated by:

$$V_{max} = Ip \cdot \sqrt{\frac{L_{leak}}{C_{lump}}}$$

where C_{lump} represents the total parasitic capacitance seen at the MOSFET opening. Typical values for Rsnubber and Csnubber in this 4W application could respectively be 1.5 kΩ and 47 pF. Further tweaking is nevertheless necessary to tune the dissipated power versus standby power.

Available Documents

"Implementing the NCP1200 in Low-cost AC-DC Converters", AND8023/D.

"Conducted EMI Filter Design for the NCP1200", AND8032/D.

"Ramp Compensation for the NCP1200", AND8029/D.

TRANSient and AC models available to download at: http://onsemi.com/pub/NCP1200

NCP1200 design spreadsheet available to download at: http://onsemi.com/pub/NCP1200

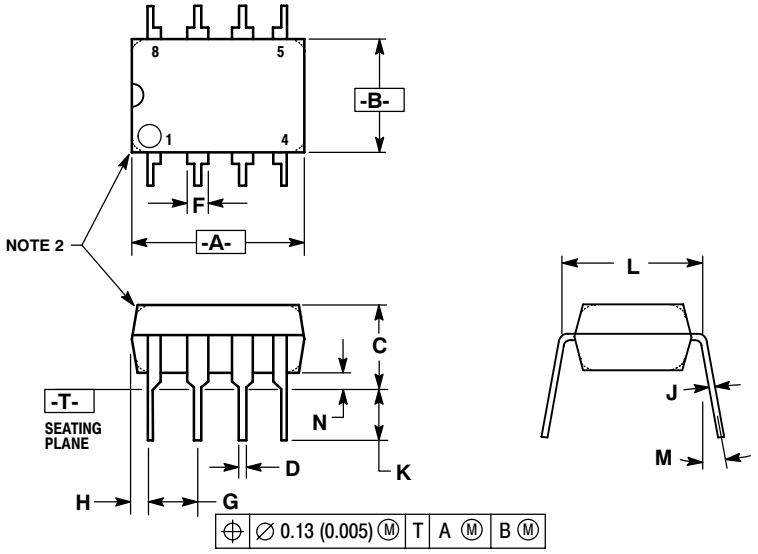
ORDERING INFORMATION

Device	Type	Marking	Package	Shipping†
NCP1200P40	F_{SW} = 40 kHz	1200P40	PDIP-8	50 Units / Rail
NCP1200P40G		1200P40	PDIP-8 (Pb-Free)	50 Units / Rail
NCP1200D40R2		200D4	SOIC-8	2500 / Tape & Reel
NCP1200D40R2G		200D4	SOIC-8 (Pb-Free)	2500 / Tape & Reel
NCP1200P60	F_{SW} = 60 kHz	1200P60	PDIP-8	50 Units / Rail
NCP1200P60G		1200P60	PDIP-8 (Pb-Free)	50 Units / Rail
NCP1200D60R2		200D6	SOIC-8	2500 / Tape & Reel
NCP1200D60R2G		200D6	SOIC-8 (Pb-Free)	2500 / Tape & Reel
NCP1200P100	F_{SW} = 100 kHz	1200P100	PDIP-8	50 Units / Rail
NCP1200P100G		1200P100	PDIP-8 (Pb-Free)	50 Units / Rail
NCP1200D100R2		200D1	SOIC-8	2500 / Tape & Reel
NCP1200D100R2G		200D1	SOIC-8 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

PDIP-8
P SUFFIX
CASE 626-05
ISSUE L



NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	---	10°	---	10°
N	0.76	1.01	0.030	0.040